

United States Patent and Trademark Office



UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION:NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/801,893	03/16/2004	Gi-ho Park	5649-1159 3389		
. 7590 04/20/2006			EXAMINER		
Robert N. Crouse			NGUYEN, THAN VINH		
Myers Bigel Sib				D. DED ARMADED	
Post Office Box 37428			ART UNIT	PAPER NUMBER	
Raleigh, NC 27627			2187		
			DATE MAILED: 04/20/2006		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application	on No.	Applicant(s)				
Office Action Summary		10/801,89	93	PARK, GI-HO				
		Examiner		Art Unit				
		Than Ngu	yen	2187				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply								
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).								
Status								
1) 🛛	Responsive to communication(s) filed on 2	27 January 200	5.					
	This action is FINAL . 2b)⊠ This action is non-final.							
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.							
Disposition of Claims								
4)🛛	☑ Claim(s) <u>1-37</u> is/are pending in the application.							
	4a) Of the above claim(s) is/are withdrawn from consideration.							
5)🛛	Claim(s) <u>29-37</u> is/are allowed.							
6)⊠	☐ Claim(s) 1-14 and 20-28 is/are rejected.							
7)🖂	Claim(s) 15-19 is/are objected to.							
8)[8) Claim(s) are subject to restriction and/or election requirement.							
Applicati	on Papers							
9) 🗆 :	The specification is objected to by the Exar	miner						
10)⊠ The drawing(s) filed on <u>16 March 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.								
,_	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority u	ınder 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.								
2) 🔲 Notic 3) 🔯 Inforr	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948 nation Disclosure Statement(s) (PTO-1449 or PTO/SE r No(s)/Mail Date 1/27/05		4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	te	O-152)			

Application/Control Number: 10/801,893 Page 2

Art Unit: 2187

DETAILED ACTION

- 1. Claims 1-37 are pending.
- 2. The IDS, filed 1/27/05, has been considered.
- 3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

- 4. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 5. Claims 14-19 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 6. As to claim 14, it is unclear with the claim language "modifying access to the DFS cache memory" mean. Without knowing what access is taking place or how the access is modified, one of ordinary skills would not be able to make and/or use the claimed invention. Claims 15-19, 25 are also rejected for incorporating the same deficiency.
- 7. As to claim 25, this claim is a system claim and depends on claim 19, a method claim. It is vague as what Applicant is claiming. Perhaps, this claim should depend on claim 20-24?
- 8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Art Unit: 2187

9. Claims 20-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This claim has undue breadth. Claim 20 is a single means claim. A single means claim which covers every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the invention. In re Hyatt, 708 F. 2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983). Claims 21-22 are similarly rejected.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 11. Claims 1-14, 20-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Shirotori et al (US 5,920,888).

As to claim 1,2,11,20,21,26,27:

12. Shirotori teaches accessing a [DFS] cache memory during an [idle] time in a [single low frequency] clock cycle (access cache using low frequency to reduce power consumption; 8/5-27; 6/21-36).

As to claim 3,12,22,28:

Art Unit: 2187

13. Shirotori teaches the idle time comprises a time interval between the completion of a high frequency DFS clock cycle and completion of a low frequency DFS cycle (Fig. 8; standby mode; 8/10-15).

As to claim 4-6,10,23-25:

14. Shirotori teaches accessing a first cache memory at a first time and second cache memory upon a miss at a second time (Fig. 8-10; accessing cache memory).

As to claim 7,13:

15. Shirotori teaches the single low frequency DFS clock cycle being a time interval between two time adjacent rising or falling DFS clock edges having no intervening clock edges (Fig. 8; 6/16-36).

As to claim 8,9:

16. Shirotori teaches the cache memory having two frequency modes (high/low access modes; Fig. 8-10; 6/20-7/5).

As to claim 14:

17. Shirotori teaches modifying access to the cache memory based on whether operating in a high or low frequency mode (Fig. 8-10; change access frequency modes to save power; 6/16-7/5).

Allowable Subject Matter

18. Claims 15-19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Application/Control Number: 10/801,893

Art Unit: 2187

19. As to claim 15, the prior art does not further teach accessing the DFS main cache memory without accessing the DFS line buffer cache memory when the DFS cache memory is operating according to the high frequency DFS clock; and accessing the DFS line buffer cache memory responsive to a miss on accessing the DFS main cache memory when the DFS cache memory is operating according to the low frequency DFS clock. Claims 16-19 are also allowable for incorporating these limitations.

Page 5

- 20. Claims 29-37 are allowed.
- 21. As to claim 29, the prior art of record does not suggest or teach nor suggest the claimed cache memory system. More specifically the prior art does not further suggest having a main cache memory configured to store main cached tag and data information; and a main cache memory enable circuit configured to disable access to the main cache memory based on a DFS signal in the on state and configured to enable access to the main cache memory during the idle time based on the DFS signal in the on state and a miss on an access to the line buffer cache memory.
- 22. As to claim 31, the prior art of record does not suggest or teach nor suggest the claimed cache memory system. More specifically the prior art does not further suggest having a main cache memory enable circuit configured to enable access to the main cache memory during an idle time in a single low frequency DFS clock cycle based on the DFS signal in the on state and a miss on the access to the tilter cache memory and configured to disable access to the main cache memory during the idle time based on the DFS signal in the on state and a hit on the access to the filter cache memory.
- 23. Claims 30,32-37 are also allowable for incorporating the limitations of the parent claim.

Art Unit: 2187

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Than Nguyen Primary Examiner

Mayer

Art Unit 2187